AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing Of Claims:

1-18. (Canceled).

19. (Currently Amended) A method for switching between at least two operating modes of a processor unit that includes at least two execution units for running programs, comprising:

assigning at least one identifier to at least the programs, the identifier allowing a differentiation between the at least two operating mode; and

switching between the operating modes as a function of the identifier such that the processor unit runs the programs according to the assigned operating mode; ~~and~~

~~comparing two input values of the at least two execution units;~~

wherein the identifier is a part of at least a program.

20. (Previously Presented) The method as recited in claim 19, wherein the programs contain task programs or constitute them, and the identifier is assigned to the corresponding individual task programs.

21. (Previously Presented) The method as recited in claim 19, wherein the programs are made up of individual program segments or contain them, and the identifier is assigned to the corresponding individual program segments.

22. (Previously Presented) The method as recited in claim 19, wherein the programs are made up of individual program instructions, and the identifier is assigned to the corresponding individual program instructions.

23. (Previously Presented) The method as recited in claim 19, wherein the programs are part of an operating system of the processor unit or constitute the operating system.

24. (Previously Presented) The method as recited in claim 19, wherein the programs are used for controlling operating sequences of a vehicle.

25. (Previously Presented) The method as recited in claim 19, wherein under the safety mode, the two execution units run identical programs redundantly.

26. (Previously Presented) The method as recited in claim 25, wherein conditions or results obtained while the programs are run are compared for agreement, errors being detected if there is a discrepancy.

27. (Previously Presented) The method as recited in claim 25, wherein the programs are run synchronously.

28. (Previously Presented) The method as recited in claim 19, wherein in the second operating mode, which corresponds to a performance mode, each execution unit runs different programs.

29. (Previously Presented) The method as recited in claim 19, wherein the identifier is in the form of at least one bit.

30. (Previously Presented) The method as recited in claim 19, wherein a program instruction provided that generates an identifier indicating if the program is to be run in the first or second operating mode.

31. (Previously Presented) The method as recited in claim 19, wherein the identifier is written to a specific memory area.

32. (Previously Presented) The method as recited in claim 31, wherein the identifier is generated by an instruction provided in an instruction set of the processor unit.

33. (Previously Presented) The method as recited in claim 32, wherein the identifier is generated by a write instruction.

34. (Currently Amended) A device for switching between at least two operating modes of a processor unit that includes at least two execution units for running programs, comprising:

an arrangement for assigning at least one identifier to at least the programs, the identifier allowing a differentiation between the at least two operating modes; and

an arrangement for switching between the operating modes as a function of the identifier such that the processor unit runs the programs according to the assigned operating mode; ~~and~~

~~a comparing arrangement to compare two input values of the at least two execution units;~~

wherein the identifier is a part of at least a program.

35. (Previously Presented) The device as recited in claim 34, further comprising: at least duplicate arithmetic-logic units provided correspondingly as at least two execution units.

36. (Currently Amended) A processor unit for running programs, comprising:

at least two execution units; and

a switching arrangement via which it is possible to switch between at least two operating modes of the processor unit, wherein[[:]] the switching arrangement assigns at least one identifier to at least the programs, the at least one identifier allowing a differentiation between the two operating modes, and the switching arrangement being designed in such a way that the switching arrangement switches between the operating modes as a function of the identifier, and the processor unit runs the programs according to the assigned operating mode; ~~and~~

~~a comparing arrangement to compare two input values of the at least two execution units;~~

wherein the identifier is a part of at least a program.

37. (New) The method as recited in claim 19, wherein the identifier includes three bits, one of the three bits indicating the operating mode and two other bits indicating a number of instruction lines that run under the operating mode.

38. (New) The method as recited in claim 19, wherein the identifier includes five bits, one of the five bits indicating the operating mode, a second and a third bits indicating a beginning line or address of a block of instructions, and a fourth and a fifth bits indicating an ending

line or address of the block of instructions, and wherein the block of instructions runs under the operating mode.